SPECIFICATION AMENDMENTS:

Please amend the paragraph beginning at page 1, line 13 as follows:

"Centralized lighting control systems are known in the art. Typically, the central computer controls the lighting system throughout a building or other facility, such as is defined by the DALI standard, a well-known lighting control standard. The lighting device being controlled interfaces to the central computer through a serial interface. A microprocessor at the lighting device usually performs ~~parallel to~~ serial to parallel conversion of incoming commands and data, error detection, and arbitration control between incoming and outgoing data and commands."

Please amend the paragraph beginning at page 1, line 19 as follows:

"Figure 1 shows typical prior art interface into a DALI control computer. The control computer 107 receives and transmits various data and commands serially over lines 103 and 104 as shown. A microprocessor 101 is employed at the lighting device to receive and process the commands and to control other elements of the lighting device over parallel bus 102. Functions executed by microprocessor 101 include error detection and correction, ~~parallel to~~ serial to parallel conversion, and edge detection, as required by the DALI standard. Control of arbitration of communications into and out of the lighting device is also implemented within microprocessor 101."

Please amend the paragraph beginning at page 2, line 23 as follows:

"The separate device is implemented in hardware to perform error detection, noise filtering, and optionally other functions previously performed by the microprocessor, such as parallel to serial conversion, serial to parallel conversion, edge detection, arbitration control, and possibly others. The hardware device interposed between the lighting device and the control computer offloads much of the functionality from the microprocessor, providing faster operating speeds and permitting better use of less expensive microprocessors typically employed at such lighting devices. In a preferred embodiment, the ~~parallel to~~ serial to parallel conversion is implemented as a preshift register and a shift register, and the error

A3

detection is implemented in common hardware with ~~parallel to~~ serial to parallel conversion."

Please amend the paragraph beginning at page 4, line 4 as follows:

A4

"Signals 214 and 215 represent the data bus exchanging data between microprocessor 202 and CPCM 201. Also in a conventional fashion, read and write signals 213 and 212, respectively, are utilized, and an interrupt signal 211 advises microprocessor 202 when the CPCM 201 wishes to transfer data. A reset signal 210 and clock signal 221 are also used conventionally. Note that preferably clock signal 221 is the same clock signal utilized for both CPCM 201 and microprocessor 202 in order to synchronize the system."

Please amend the paragraph beginning at page 4, line 23 as follows:

A5

"Figure 3 represents a more detailed hardware diagram to implement the functions of error detection, serial to parallel conversion, edge detection and arbitration control for signals entering and exiting from the CPCM 201. ~~The~~ A host interface ~~310~~ transmits and receives parallel data over a PC conventionally."

Please amend the paragraph beginning at page 5, line 3 as follows:

A6

'In operation, data is received serially from the control computer and entered into a preshift register 301. The error detection noise filtering and ~~parallel to~~ serial to parallel conversion is implemented in conjunction with the pre-shift and shift registers 301 and 302, respectively. The error detection is a hardware circuit 313 that detects particular bit patterns in the incoming data, which violate rules of parity or other error detection techniques.

Please amend the paragraph beginning at page 5, line 15 as follows:

A7

"Additionally, the start of data is noted in the DALI Standard by a falling edge which is also detected by an edge detect circuit 304, and conveyed to an arbitration control logic 306. The arbitration control logic 306 ensures that data being held in locations 321 through 327 is not overwritten by new data before it is read out by the

microprocessor. Conventional logic may be used to implement such a system wherein no new data is rewritten into any register 321 through 327 until the previous data is read out. A clock divider 340 serves to operate the CPCM 201 at a rate sufficient to allow for the parallel to serial conversion. "

Please amend the paragraph beginning at page 5, line 22 as follows:

'Registers 321 through 327 are special function registers. Register 321 is the clocking register and is used to set or adjust the data rate in order to provide for signals being read and written to and from the microprocessor and the control computer at different rates. More specifically, the ~~parallel to~~ serial to parallel conversion requires that the serial interface operate at many times the speed of the parallel interface in order to keep up with data being sent in parallel."

Please amend the paragraph beginning at page 6, line 10 as follows:

"In operation, serial data arrives ~~by~~ via line 351 and is shifted into preshift register 301. The data is not shifted into register 302 until it has been verified as correct via the error detection and P/S control block 303. Since the preshift register 301 is typically smaller that the shift register 302, the data from the preshift register 301 will be shifted to the shift register 302 plural times for each readout from the shift register 302. The error detection is performed in the smaller preshift register 301, and the data is only shifted to shift register 302 after passing the error detection testing in preshift register 301. Hardware device 303 is an error detection system which will substantially immediately detect signaling errors should such an error occur. The generation of such an error will be signaled back to the control computer, and the DALI protocol provides for the retransmission of such erroneously transmitted signals."